Application No.: 10/758,311 Docket No.: 65783-0038

## AMENDMENTS TO THE CLAIMS

1. (Original) A system for controlling a dual-speed motor comprising:

a direct current (DC) power supply;

a dual-speed DC motor;

a first solid-state switch electrically coupled to said DC power supply and a low-speed input of said dual-speed DC motor;

a second solid-state switch electrically coupled to said DC power supply and a high-speed input of said dual-speed DC motor; and

a third solid-state switch electrically coupled between said first solid-state switch and said low-speed input of said dual-speed DC motor, wherein a first side of said third solid-state switch is coupled to a power supply side of said system and a second side of said third solid-state switch is coupled to a load side of said system.

2. (Original) The system of claim 1, wherein said first and second solid-state switches comprise intelligent solid-state switches.

3. (Original) The system of claim 1, wherein said third solid-state switch comprises one of a
power metal oxide semiconductor field effect transistor (MOSFET) or an insulated gate bipolar transistor (IGBT).

4. (Original) The system of claim 1, wherein said DC power supply comprises a 14 volt battery.

5. (Original) The system of claim 1, further comprising:

a microcontroller including a low-speed control channel and a high-speed control channel electrically coupled to said first, second, and third solid-state switches;

wherein said high-speed control channel is electrically coupled to said second solid-state switch; and

wherein said low-speed control channel is electrically coupled to said first solid-state switch and said third solid-state switch.

6. (Original) The system of claim 5, further comprising:

a first transistor electrically coupled between said low-speed control channel and said first solid-state switch; and

a second transistor electrically coupled between said high-speed control channel and said second solid-state switch.

7. (Original) The system of claim 6, wherein said first and second transistors comprise bipolar junction transistors (BJT).

8. (Original) The system of claim 6, further comprising a third transistor electrically coupled between said low-speed control channel and said third solid-state switch.

9. (Original) The system of claim 6, further comprising a gate driver electrically coupled between said low-speed control channel and said third solid-state switch.

10-14. (Cancelled)

15. (Original) A system for controlling a dual-speed motor comprising:

a means for supplying power;

a dual-speed DC motor;

a first means for switching electrically coupled to said power supplying means and a low-speed input of said dual-speed DC motor;

a second means for switching electrically coupled to said power supplying means and a high-speed input of said dual-speed DC motor; and

a third means for switching electrically coupled between said first switching means and said low-speed input of said dual-speed DC motor, wherein a first side of said third switching means is coupled to a power supply side of said system and a second side of said third switching means is coupled to a load side of said system.

16. (Original) The system of claim 15, wherein said third switching means comprises a solid-state switch.

17. (Original) The system of claim 15, further comprising:

a means for controlling said first, second, and third switching means;

wherein said controlling means is configured to selectively activate said first, second, and third switching means.

18. (Original) A method for providing a dual-speed direct current (DC) motor having reduced sneak path comprising:

providing a dual-speed DC motor and a DC power supply, wherein said dual-speed DC motor and said DC power supply are electrically coupled;

providing a first solid-state switch coupled between said DC power supply and a high-speed terminal of said dual-speed DC motor;

providing a second solid-state switch coupled between said DC power supply and a low-speed terminal of said dual-speed DC motor;

providing a third solid-state switch coupled between said second solid-state switch and said low-speed terminal of said dual-speed DC motor; and

arranging said third solid-state switch coupled between said second solid-state switch and said low-speed terminal of said dual-speed DC motor such that said third solid-state switch prevents a sneak current from passing to said second solid-state switch.

19. (Original) The method of claim 18, wherein said step of arranging said third solid-state switch comprises:

electrically coupling a first side of said third solid-state switch to said second solid-state switch; and

electrically coupling a second side of said third solid-state switch to said low-speed terminal of said dual-speed DC motor.

20. (Original) The method of claim 19, wherein said first and second solid-state switches comprise intelligent solid-state switches.

21. (Original) The method of claim 19, wherein said third solid-state switch comprises one of a power metal oxide semiconductor field effect transistor (MOSFET) or an insulated gate bipolar transistor (IGBT).

22. (Original) The method of claim 19, further comprising:

providing a microcontroller including a low-speed control channel and a high-speed control channel electrically coupled to said first, second, and third solid-state switches;

wherein said high-speed control channel is electrically coupled to said second solid-state switch; and

wherein said low-speed control channel is electrically coupled to said first solid-state switch and said third solid-state switch.

23. (Original) The method of claim 22, further comprising:

electrically coupling a first transistor between said low-speed control channel and said first solid-state switch; and

electrically coupling a second transistor between said high-speed control channel and said second solid-state switch.

24. (Original) The method of claim 23, wherein said first and second transistors comprise bipolar junction transistors (BJT).

25. (Original) The method of claim 23, further comprising electrically coupling a third transistor between said low-speed control channel and said third solid-state switch.

26. (Original) The method of claim 23, further comprising electrically coupling a gate driver between said low-speed control channel and said third solid-state switch.